The listing of claims will replace all prior versions, and listings, of claims in the present application:

LISTING OF CLAIMS:

Claim 1 (Currently Amended) A method for compensating threshold voltage roll-off within a semiconductor chip or system comprising ~~the steps of~~:

designing a semiconductor chip or system having a plurality of transistor devices in which ~~the~~ channel length of each transistor device is equal to L_{nom};

setting off-current of each transistor device to I-off_{max} by predetermining that each transistor device has a channel length equal to L_{max} and then implanting into each channel of each transistor device such that its threshold voltage is equal to Vt_{min};

testing ~~the~~ off-current of each transistor device; and

biasing the ~~back-gate~~ back gate or ~~the~~ body nodes of some transistor devices, each of which has ~~that have~~ an off-current that does not meet a preselected specification of about I-off_{max}, to increase ~~the~~ threshold voltage of each of said transistor devices to about Vt_{min} thereof thereby compensating the threshold voltage roll-off within said semiconductor chip or system.

Claim 2 (Original) The method of Claim 1 wherein L_{nom} is 25 nm.

Claim 3 (Currently Amended) The method of Claim 1 wherein the setting off-current ~~setting~~ is controlled by varying implant conditions and ion dosage.

Claim 4 (Currently Amended) The method of Claim 3 wherein the implanting is performed at an energy from about 5 keV to about 30 keV.

Claim 5 (Currently Amended) The method of Claim 3 wherein the ion dosage for a p-type dopant is from about 1E11 atoms/cm^2 to about 1E14 atoms/cm^2.

Claim 6 (Currently Amended) The method of Claim 3 wherein the ion dosage for an n-type dopant is from about 1E11 atoms/cm^2 to about 1E14 atoms/cm^2.

Claim 7 (Original) The method of Claim 3 wherein the implanting comprises a p-type dopant selected from ions of Group III elements.

Claim 8 (Original) The method of Claim 3 wherein the implanting comprises an n-type dopant selected from ions of Group V elements.

Claim 9 (Currently Amended) The method of Claim 1 wherein the biasing occurs after manufacturing of the semiconductor chip or system during the testing thereof.

Claim 10 (Currently Amended) The method of Claim 1 wherein the biasing occurs at a time after manufacturing of the semiconductor chip or system and after the testing thereof.

Claim 11 (Original) The method of Claim 1 wherein the biasing is achieved by an external DC voltage source.

Claim 12 (Currently Amended) The method of Claim 1 wherein the biasing is achieved by an internal circuit that can deliver a potential to the back gate ~~back-gate~~ or the body nodes of ~~the second~~ some transistor devices.

Claim 13 (Currently Amended) The method of Claim 1 wherein the biasing is achieved by an external clock system that can deliver a potential.